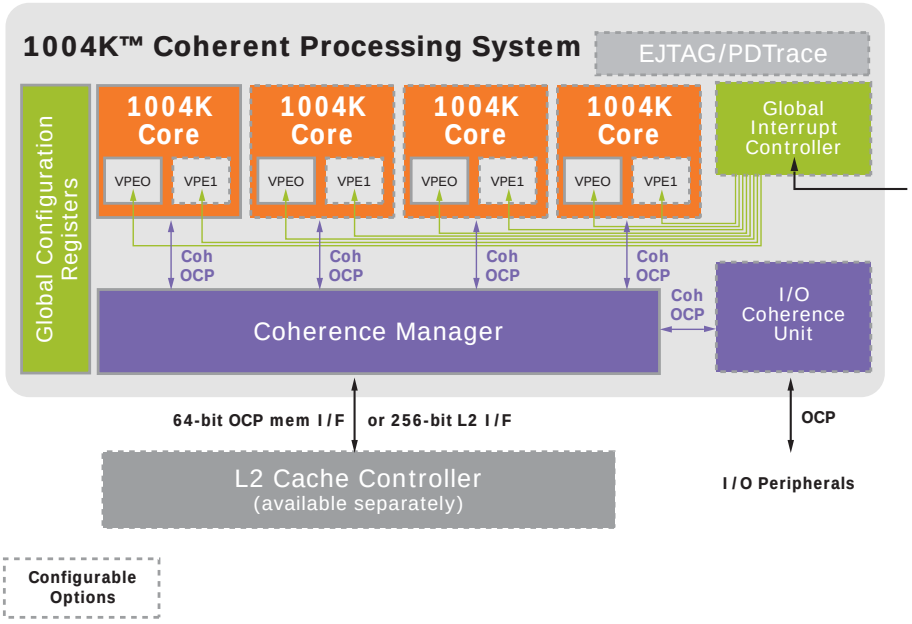
MIPS32® 1004K™

Industry's first multi-threaded multiprocessor IP core for embedded applications

The MIPS32® 1004K™ Coherent Processing System (CPS) is the next advance in licensable processing technology from MIPS Technologies. The 1004K CPS is a highly scalable multiprocessor platform that supports up to four cores connected via a coherent system architecture. Through the inclusion of hardware multi-threading in each core, the 1004K CPS is optimized to maximize performance in System-on-Chip (SoC) implementations and overcome historical performance limitations in embedded systems due to memory constraints and access latencies.



Baseline Specifications (Preliminary)

Product	MIPS32® 1004K™ core
Process	TSMC 65GP
Frequency (MHz) (worst case)	>800
Performance DMIPS/MHz	1.5/core
Total Area*	~4.2mm²

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process, and cell libraries

Quoted speeds are PTSI and don't contain OCV, clock jitter or design margin

*Configuration: 2 cores, each core with 2 threads/core and 32KB Inst/Data caches, Coherence Manager (CM), and Global Interrupt Controller (GIC)

Key Applications

Digital Home:

- Enhanced set-top boxes (STBs)
- HD digital consumer multimedia
- Residential gateways (RGWs)

Enterprise Communications Infrastructure

Network Attached Storage (NAS)

Office Automation/Multi-Function Products (MFPs)

- Medium/large office print/fax/scan

MIPS32 1004K CPS Highlights

- A coherent multiprocessor system using multi-threading to extend performance beyond traditional multiprocessor solutions
  - Up to four multi-threaded CPU cores, with two hardware threads/core
  - Multi-threading complements multi-core – leverages SMP operating systems and programming models, with minimal silicon cost adder
- Hardware I/O coherency – offloads CPU software I/O coherency overhead
- Configuration and scalability at core and system levels, addressing a broad range of price/performance implementation points for optimal product implementations
- Licensable IP core – enables broad industry adoption

Features

A complete system for coherent multiprocessing, including:

- 1 to 4 1004K multi-threaded "base" cores (up to 8 hardware threads)
- Coherence Management (CM) unit – the system "glue" for managing coherent operation between cores and I/O
- I/O Coherence Unit (IOCU) – hardware block for offloading I/O coherence from software implementation on CPUs
- Global Interrupt Controller (GIC) – system and inter-processor interrupt controller
- Extended 256-bit interface to L2 cache controller (available separately)
- EJTAG/PDtrace™ block for advanced debug/trace of complete coherent system

1004K Base Core

- 9-stage pipeline delivering more than 1.5 DMIPS/MHz per core
- Supports single- or dual-threaded operation per core
- Uses Virtual Processing Elements (VPEs) for hardware multi-threading
- Integer (1004Kc™) and floating point (1004Kf™) versions
- Support for Revision 1 of MIPS32 DSP ASE
- Coherency port has duplicate data cache tags for background coherency checks
- Design-time configurability for inclusion and sizing of instruction and data TLBs, caches, scratchpad RAM and other options

Floating Point Unit (FPU)

- IEEE 754-compliant FPU, compliant to MIPS® 64-bit FPU architecture (1004Kf version only)
- Supports single- and double-precision data types
- Separate in-order, dual-issue pipeline decoupled from integer pipeline

Coherency Management (CM) Unit

- Manages coherency using the MESI protocol
- Operates at same clock (1:1) as CPUs for maximum performance
- 256-bit extended interface for maximum throughput to (optional) L2 cache controller
- Supports performance enhancements via L1 cache-to-cache transfers, speculative reads to external memory, and globalized cache operations
- Global Configuration Registers (GCRs) for configuring/controlling CM scheme

I/O Coherence Unit (IOCU) – optional use

- Bridges non-coherent I/O peripheral transfer and makes transactions coherent
- Supports per-transaction attributes for snooping L1 caches, L1+L2 caches, or non-coherent transactions, plus I/O prioritization

Global Interrupt Controller (GIC) – optional use

- Supports system-level interrupts; inter-processor interrupts
- Routes interrupts to particular core or VPE
- Configurable # of system interrupts (up to 256)

Development Tools

- MIPS Navigator™ ICS - IDE, software toolkit, MIPSsim™, EJTAG and PDtrace probes
- CodeSourcery - SG++ toolchains for MIPS

Uses multi-threading to deliver maximum performance from each core

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